RESEARCH ARTICLE

Embedded Multi-Core Gyro Attitude Data Acquisition System for Aerospace Vehicle Based on ZYNQ Platform

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Abstract

Aiming at the interrupt storm performance bottleneck existing in high-speed gyro attitude signal acquisition of aerospace vehicles, an embedded heterogeneous multi-core data acquisition system based on Xilinx ZYNQ-7000 SoC is proposed for inertial measurement unit (IMU) gyro signal sampling. On the hardware layer, a sensor data interface IP conforming to AXI4-Stream protocol is designed in programmable logic (PL) to collect high-frequency gyro original signals, and an AXI DMA controller builds a wideband direct peripheral-DDR transmission channel to realize zero-copy data writing, greatly reducing processor resource occupation under continuous inertial attitude sampling. On the software layer, an AMP dual-core bare-metal parallel framework is deployed in the processing system (PS): the main core undertakes real-time DMA scheduling and hardware interrupt response for gyro sampling streams, while the auxiliary core independently completes attitude data packaging and external communication transmission, thoroughly decoupling high-speed inertial signal acquisition and low-rate data interaction. Meanwhile, an inter-core communication (IPC) mechanism with ultra-low 1.5 μs delay is constructed based on on-chip memory (OCM) and spinlock algorithm to guarantee multi-core consistency of gyro attitude data. Closed-loop hardware-software joint verification shows that the system supports lossless gyro data transmission at 2 MB/s under 500 kSPS high sampling rate with zero packet loss; the channel inherent noise is measured at 2.4 mV, well within the 5 mV specification threshold, which meets the high real-time and high-precision measurement requirements of aerospace vehicle inertial gyro attitude sensing, and verifies the engineering advantages of this heterogeneous multi-core architecture in aerospace inertial measurement.

Keywords: ZYNQ SoC, aerospace inertial measurement, gyro attitude data acquisition, Asymmetric Multi-Processing (AMP), AXI DMA, Inter-Processor Communication (IPC), spin lock.

1 Introduction

High-speed and high-precision data acquisition (DAQ) equipment is the core sensing hardware of aerospace vehicle inertial measurement systems, which is

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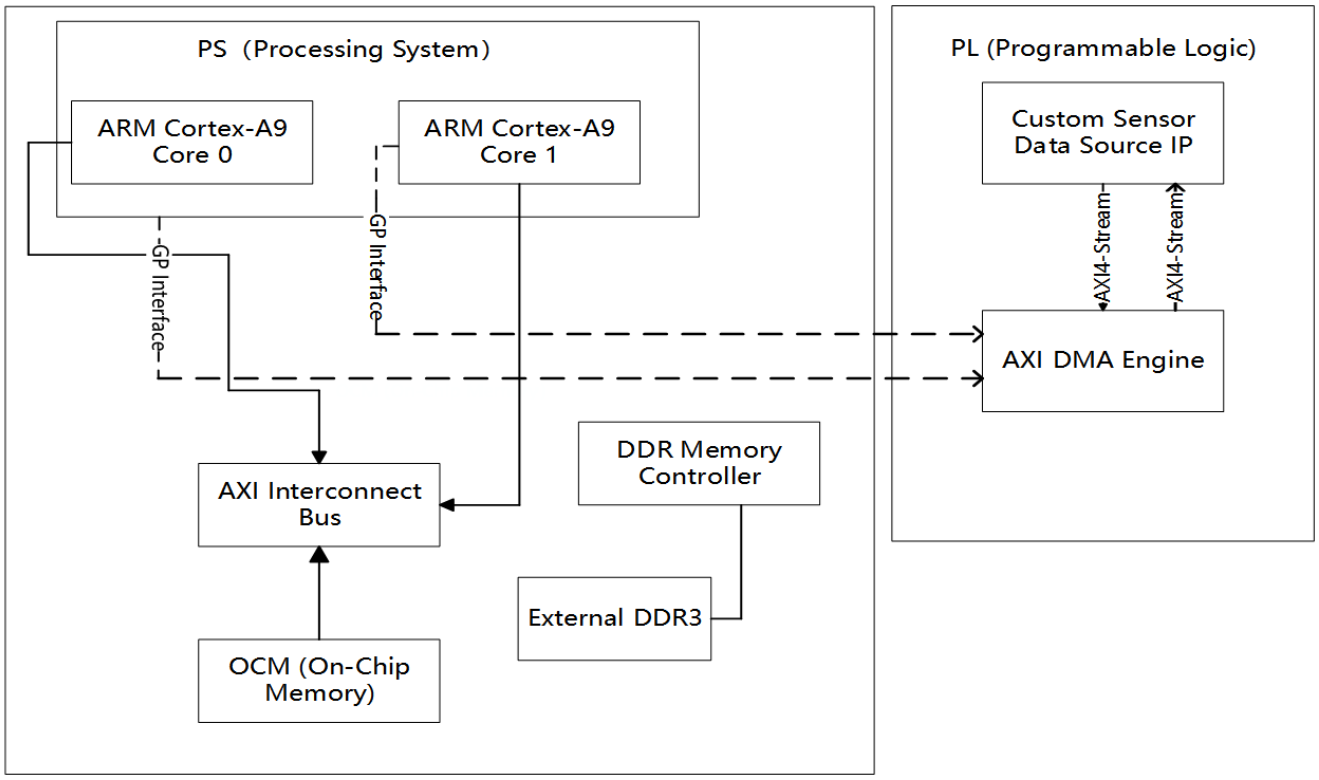


Figure 1. Block Diagram of ZYNQ PS-PL Heterogeneous Co-working Framework.

responsible for real-time collection of gyroscope attitude signals to support flight attitude solving, orbit control and stable platform control tasks. Traditional single-chip microcontroller-based inertial sampling systems face prominent performance defects when synchronously processing high-frequency gyro raw sampling streams and multi-channel telemetry communication tasks. Frequent task context switching and concurrent peripheral requests easily trigger interrupt storms, which damage the real-time certainty of gyro attitude data, leading to frame loss of inertial measurement data, compromising the accuracy of attitude computation, and ultimately resulting in erroneous flight state estimation of the vehicle.

To break through the above engineering limitations, field programmable gate arrays (FPGAs) are widely applied in real-time inertial navigation and measurement systems, as demonstrated by FPGA-based embedded navigation platforms integrating inertial sensors with GPS for real-time positioning solutions [8]. However, pure FPGA single-layer design lacks flexible upper-layer telemetry protocol analysis and complex flight task scheduling ability. In contrast, multi-core processors running symmetric multiprocessing (SMP) operating systems have unpredictable task scheduling delay, which cannot satisfy the hard real-time index of gyro attitude acquisition. Therefore, realizing physical layer task separation between time-sensitive gyro inertial sampling and non-real-time flight data communication has always been a key difficulty in aerospace inertial measurement equipment development.

This paper designs an embedded heterogeneous multi-core gyro attitude data acquisition system oriented to aerospace vehicles based on Xilinx ZYNQ-7000 SoC. High-precision multi-channel data acquisition front-ends remain a foundational engineering concern across sensing platforms, as demonstrated by dedicated acquisition system designs for capacitive and inductive sensing applications [1]. In the programmable logic (PL) layer, a customized AXI4-Stream [11] gyro sensor interface and AXI DMA high-speed transmission engine are developed to build a zero-copy direct storage path for inertial attitude data to DDR memory. In the processing system (PS) layer, an asymmetric multi-processing (AMP) bare-metal operation framework is built to separate underlying gyro DMA scheduling and upper telemetry communication functions. In addition, an OCM + spinlock-based inter-core communication mechanism is designed to ensure synchronous consistency of multi-core gyro attitude measurement data. Multiple groups of closed-loop contrast experiments prove that the system can continuously

output 2 MB/s complete gyro inertial data with zero packet loss under 500 kSPS sampling rate, which has strong stability and reliability for long-term aerospace inertial attitude measurement tasks.

2 System Architecture and Hardware Design

The overall topology of the proposed heterogeneous gyro attitude acquisition system is integrated on a single ZYNQ-7000 SoC chip [5], which physically separates hardware-driven high-speed gyro inertial sampling and software-based flight attitude data processing control. Figure 1 illustrates the overall co-working framework between the PS and PL, highlighting the data flow from the gyro sensor interface through the AXI DMA to the DDR memory, and the subsequent processing by the dual-core AMP system.

2.1 Custom Sensor Interface and AXI4-Stream Packing

A dedicated peripheral interface IP core is developed by Verilog in programmable logic (PL), which drives a 16-bit dual-channel high-precision ADC (ADS8354, with a maximum sampling rate of 700 kSPS) to complete gyro analog attitude signal collection at a configured 500 kSPS sampling rate. The serial raw bitstream output by the inertial gyro is parallelized and encapsulated into standard 32-bit AXI4-Stream data format under 100 MHz global clock. This packetized streaming approach to high-frequency sensor data transmission follows established design principles from multi-channel acquisition architectures, such as those developed for high-frequency ground wave radar systems requiring robust acquisition and transmission protocols [3]. To reduce bus handshake overhead and divide effective data transmission boundaries, a hardware packetizer is integrated into the gyro sensor interface module. It monitors real-time inertial sampling streams and automatically pulls up the TLAST end signal every 32 data words (128 bytes). This hardware-level data segmentation splits continuous high-speed gyro attitude signals into fixed-length standard data packets, providing accurate packet end identification signals for downstream DMA data transmission.

2.2 High-Speed DMA and HP0 Memory Mapping

To completely eliminate CPU data forwarding overhead during mass gyro attitude data transmission, AXI DMA is selected as the core high-bandwidth memory access channel. Zynq-based high-bandwidth acquisition architectures have demonstrated reliable performance in demanding field deployments, such as remote seismic data acquisition stations operating under extreme environmental constraints [2]. The DMA is configured as unidirectional S2MM storage mode with burst length set to 16; its memory mapping master interface is connected to ZYNQ PS high-performance port S_AXI_HP0 through AXI SmartConnect interconnect. The S_AXI_HP0 port provides an exclusive high-bandwidth bus channel for external DDR3 storage. This hardware pipeline realizes zero-copy direct memory writing of gyro inertial data, and mass continuous attitude sampling data can be automatically cached to pre-allocated memory buffers without occupying any core operation cycles.

3 Software Framework and Multicore Synchronization

The processing system (PS) adopts asymmetric multiprocessing (AMP) architecture with two bare-metal ARM Cortex-A9 cores [7] to realize rigid functional division for aerospace gyro attitude measurement tasks. This dual-core task-separation philosophy is consistent with AMP-based controller designs in other real-time embedded domains, where heterogeneous operating environments across cores have been shown to effectively decouple time-critical and non-critical processing tasks [4].

```
void uart_lock() {
    while (Xil_In32(UART_LOCK_ADDR) == 1) {
    }
    Xil_Out32(UART_LOCK_ADDR, 1);
}
void uart_unlock() {
    Xil_Out32(UART_LOCK_ADDR, 0);
}
```

Figure 2. Underlying implementation of spinlock.

3.1 AMP Dual-Core Architecture and Memory Isolation

To avoid shared resource conflict and bus congestion during multi-core joint processing of gyro inertial data, the total 1 GB DDR3 physical address space is strictly divided by linker script lscript.ld. Core 0 occupies the lower 256 MB memory area, which is fully responsible for underlying gyro DMA buffer scheduling and high-frequency inertial sampling hardware interrupt response (S2MM interrupt signal cascaded through IRQ_F2P). Core 1 runs independently in the upper 768 MB memory space, and its tasks include gyro attitude data digital filtering, inertial measurement packet

reorganization and external aerospace telemetry protocol communication interaction.

3.2 Cache Coherency Management

The PL-side AXI DMA writes gyro sampling data directly into the physical DDR memory, bypassing the CPU-internal SCU snoop control unit. Consequently, Core 1's L1/L2 caches may retain stale copies of the inertial attitude data, leading to cache lag and erroneous retrieval of gyro measurement values.

To resolve this multi-core data inconsistency, Core 1 performs an immediate cache invalidation operation upon receiving a new gyro buffer update notification:

```
Xil_DCacheInvalidateRange((INTPTR)DmaRxBuffer,
MAX_DMA_LEN);
```

This instruction forces Core 1 to invalidate the outdated cache lines and subsequently reload the latest gyro raw attitude data directly from the external DDR memory, ensuring data coherence between the DMA-updated memory and the CPU's cache hierarchy.

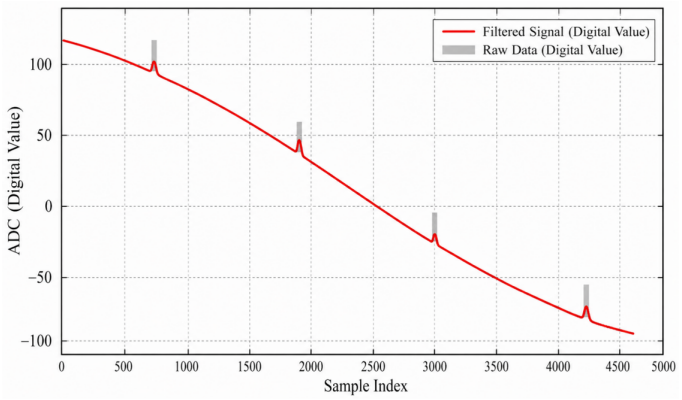
3.3 OCM-Based Inter-Processor Communication and Spinlock

Core 0 and Core 1 transmit gyro data buffer pointers through a lightweight communication protocol built in unbuffered on-chip memory (OCM), and the inter-core synchronization delay is controlled below 1.5 μs. However, both cores share the UART1 peripheral for aerospace equipment status debugging output; simultaneous printing operations will cause garbled gyro log information or even system deadlock. To realize access mutual exclusion of shared peripherals, drawing on established scalable synchronization algorithms for shared-memory multiprocessor systems [10], an atomic spinlock variable is allocated at OCM address 0xFFFF0014:

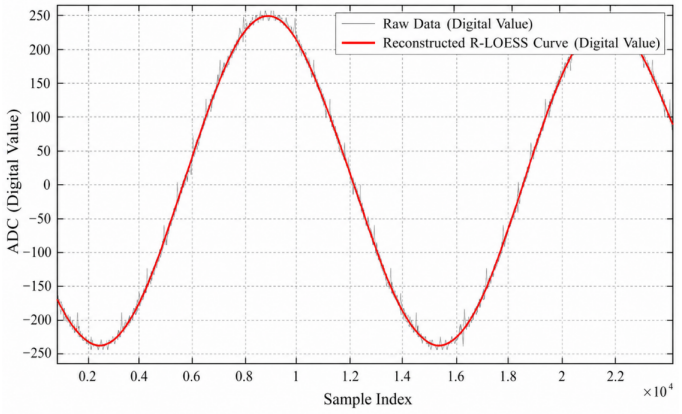
Figure 2 depicts the underlying implementation of the spinlock mechanism, which relies on atomic test-and-set operations to ensure mutually exclusive access to shared resources like the UART peripheral. Relying on this hardware-supported mutual exclusion loop mechanism, the resource competition problem of dual-core during aerospace gyro attitude data processing is completely eliminated.

4 Experimental Results

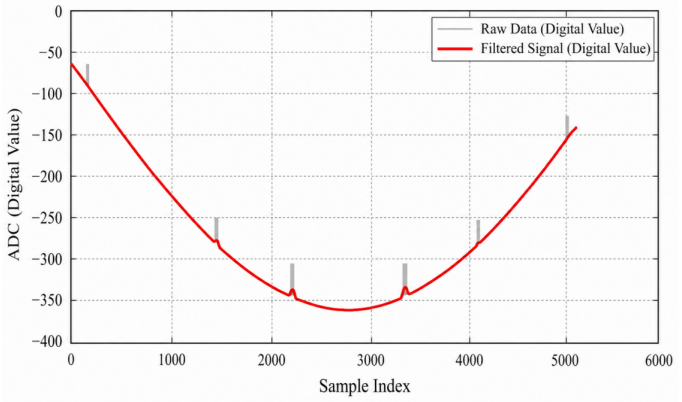
A closed-loop test platform for aerospace inertial measurement is built to comprehensively evaluate the real-time performance of the ZYNQ gyro attitude



a) 8kHz/250mVpp



b) 8kHz/500mVpp

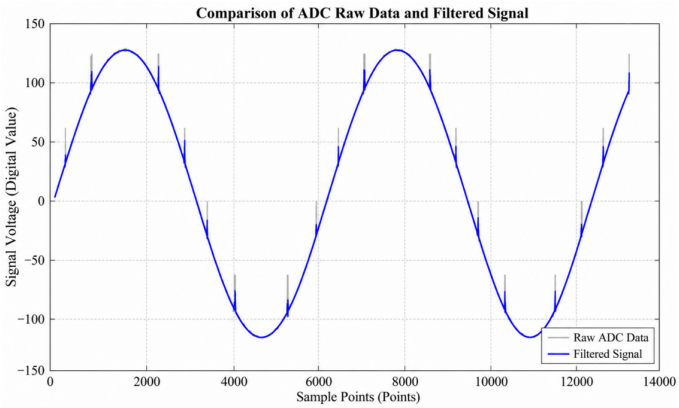


c) 8kHz/750mVpp

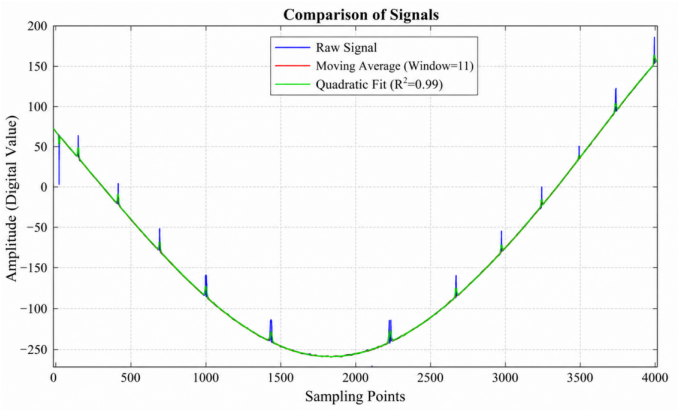
Figure 3. 8 kHz Sinusoidal Excitation: Acquisition, Filtering and Waveform Reconstruction.

acquisition system proposed in this paper. An arbitrary waveform generator (AWG) simulates the analog weak output signal of aerospace MEMS gyroscope. Cross contrast testing is carried out by changing input signal amplitudes (250 mVpp, 500 mVpp, 750 mVpp) and signal frequencies (8 kHz, 16 kHz, 32 kHz) to simulate different dynamic attitude working conditions of aircraft.

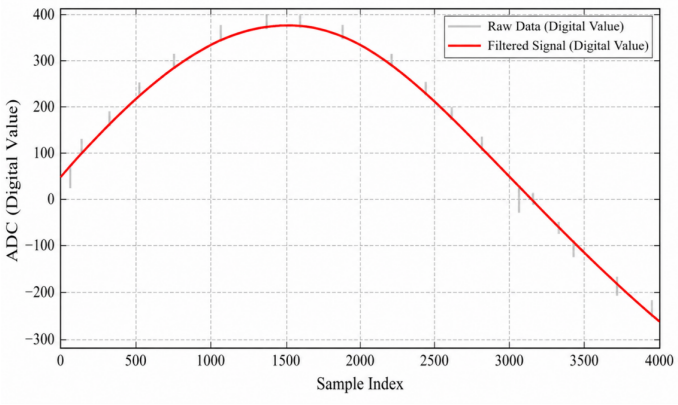
Time-domain waveform analysis shows that the raw gyro sampling data contains obvious analog



a) 16kHz/250mVpp

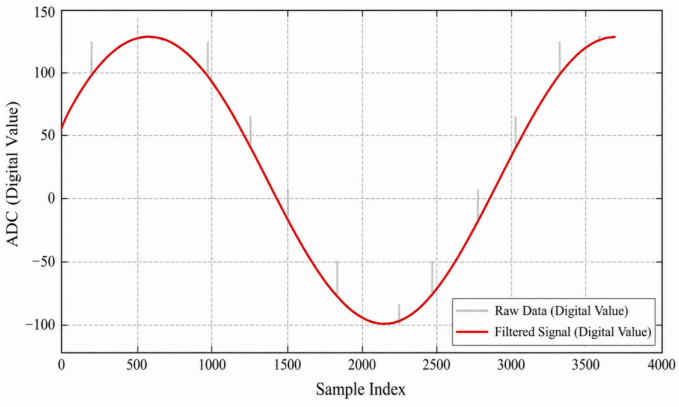


b) 16kHz/500mVpp

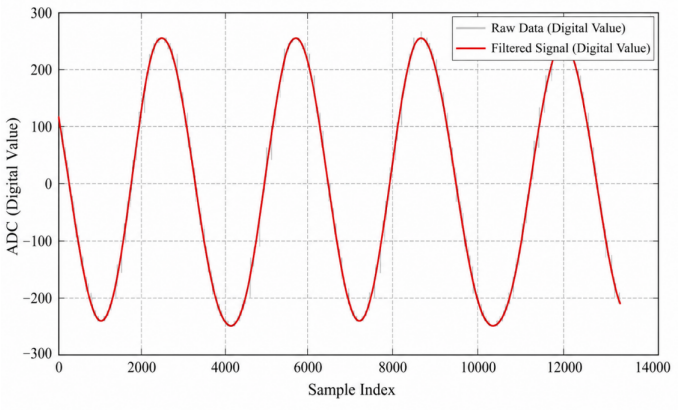


c)16kHz/750mVpp

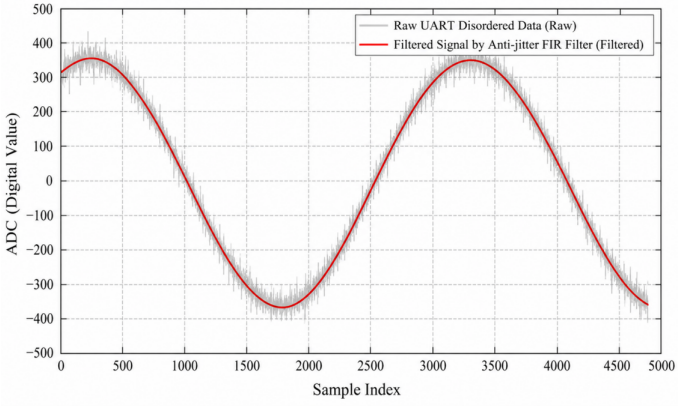
Figure 4. 16 kHz Sinusoidal Excitation: Acquisition, Filtering and Waveform Reconstruction.



a)32kHz/250mVpp



b)32kHz/500mVpp



c)32kHz/750mVpp

Figure 5. 32 kHz Sinusoidal Excitation: Acquisition, Filtering and Waveform Reconstruction.

front-end inherent noise, consistent with characteristic MEMS gyroscope noise behavior reported in prior inertial sensor studies [9]. After adopting the designed cascaded digital filtering algorithm (moving median filtering combined with Savitzky-Golay smooth filtering [6]), the reconstructed gyro attitude signal can accurately restore high-frequency motion waveform without phase offset and harmonic distortion.

Figure 3 presents the acquisition, filtering, and waveform reconstruction results for an 8 kHz sinusoidal excitation. The raw signal exhibits significant high-frequency noise, but the filtered output clearly recovers the fundamental 8 kHz component with excellent phase alignment and amplitude fidelity, demonstrating the effectiveness of the cascaded filtering algorithm at lower frequencies.

Figure 4 shows the results for a 16 kHz sinusoidal excitation. Even as the input frequency doubles, the system maintains accurate signal reconstruction. The filtered waveform tracks the input precisely, and the noise floor remains well-suppressed, indicating

Table 1. Quantitative performance of the heterogeneous aerospace gyro attitude acquisition system.

evaluation parameter	specification	measured	status
gyro sampling rate	500 kSPS	500 kSPS	qualified
continuous inertial data throughput	> 1.5 MB/s	2.0 MB/s	qualified
gyro data packet loss rate	0%	0%	qualified
channel baseline noise	< 5 mV	2.4 mV	excellent
signal-to-noise ratio of gyro measurement	> 70 dB	74.2 dB	high-fidelity
spurious-free dynamic range	> 80 dB	85.4 dB	high-fidelity

that the data acquisition channel and filtering algorithms perform consistently well within the intended operational bandwidth.

Figure 5 depicts the most challenging test case with a 32 kHz sinusoidal excitation, representing the upper boundary of the intended gyro signal measurement bandwidth in this system. At this frequency, which corresponds to approximately 6.4% of the Nyquist frequency (250 kHz) under the 500 kSPS sampling rate, the acquisition channel and filtering pipeline operate under relatively demanding signal conditions within the designed operational range. Despite the increased dynamic demands, the reconstructed signal shows no significant phase distortion or amplitude attenuation. The close match between the filtered output and the ideal sine wave confirms the system's capability to handle high-frequency gyro attitude signals with high fidelity, which is critical for capturing rapid aerospace vehicle maneuvers.

Under full-load stress test with 1,000,000 consecutive gyro sampling points, the data packet serial number increases strictly monotonically, which verifies zero loss of inertial attitude data packets. The quantitative performance indicators of the aerospace inertial acquisition system are summarized in Table 1.

5 Conclusion

This work demonstrates that the interrupt-storm bottleneck inherent to single-core gyro acquisition can be structurally eliminated, rather than merely mitigated, by physically separating time-critical sampling from non-critical communication at the PS-PL hardware boundary: zero-copy DMA removes CPU involvement from the data path, while bare-metal AMP partitioning removes scheduling uncertainty from the control path, and neither alone would have satisfied the hard real-time requirement under sustained 500 kSPS sampling. The present validation, however, relies on laboratory AWG-simulated gyro signals under controlled bench conditions, so translating these results to flight-representative environments will require further characterization under mechanical vibration, thermal cycling, and electromagnetic interference, which are known to perturb both ADC front-end noise and OCM synchronization timing; the current spinlock-based IPC mechanism may also require reconsideration if the architecture is extended beyond two cores, as contention typically scales poorly with core count. Future work will therefore proceed toward ruggedization testing under representative aerospace environmental conditions and architectural extension to multi-axis IMU fusion, which will require evaluating whether the present dual-core task allocation remains adequate or whether a three-core or quad-core AMP partition becomes necessary to accommodate additional sensor fusion and real-time attitude-solving workloads.

Data Availability Statement

Data will be made available on request.

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Conflicts of Interest

The authors declare no conflicts of interest.

AI Use Statement

The authors declare that DeepSeek-R1 was used for translation and proofreading of the entire manuscript. The authors have reviewed and edited the output and take full responsibility for the content of the manuscript.

Ethical Approval and Consent to Participate

Not applicable.

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